EE 410 PROJECT REPORT

- HIGH EFFICIENCY HEADPHONES AMPLIFIER -

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1 PROJECT ABSTRACT

The purpose of this project was to design a stereo headphones amplifier to meet a given set of specifications. The project was launched in the form of an EE 410 design competition with the overriding goal of minimizing power consumption while meeting all of the specifications. This report documents the circuit design and analysis performed by the team that produced the most efficient headphones amplifier. The winning design features a near- rail-to-rail output stage driven by a voltage amplifier with slightly higher supply rails. The amplifiers are biased in the class B region and fundamentally configured to operate from a single supply. The complete application is powered by two AAA alkaline batteries and employs three dc-dc switching converters to produce the necessary voltages to deliver 100mW audio power per channel to each 32Ω load. The final measured efficiency at max output power was 54%, with 23% of power being dissipated in the class B amplifiers, and the remaining 23% being lost in the dc-dc converter circuitry.

2 PROJECT SPECIFICATION

The headphones amplifier was designed to satisfy the following specifications:

Parameter	Min	Typ	Max	Units	Comment
Input Characteristics:					
Input Impedance		10 k		Ω	
Input level		−10	0	dBV	0 dBV = 1 V_{RMS}
Connector		1/8" stereo mini-jack			3-conductor
Output Characteristics:					
Maximum Output Level	100			mW	Without clipping
Rated Load Impedance		32		Ω	Typ. headphone Z
Output Impedance			3.2	Ω	Damping factor of 10
Connector		1/8" stereo mini-jack			3-conductor
Overall Characteristics (End-to-end measurement):					
Frequency Range	20		20 k	Hz	
Frequency Response			±1.0	dB	
Nominal Gain		20		dB	See note 1
Gain Adjustment Range	30			dB	See note 1
*THD			0.1	%	At 10 mW; see note 2
			1.0	%	At 100 mW; see note 2
Noise Density at output			−128	dBV/ $\sqrt{Hz}$	See note 3
Power Requirements:					
Power Source		2 AAA cells			Alkaline batteries
Input Voltage			3	VDC	Consider voltage variation vs. time
*Power Consumption			400	mW	See note 4
*Battery Life	90			hours	See note 5
Cost:					
*Materials cost			$40		

FIGURE 1- HEADPHONES AMPLIFIER SPECIFICATIONS

Other than the specifications listed above, we were given complete freedom in our design. For the competition aspect, we tried to minimize the power consumption and materials cost. With that in mind, our primary objectives were to minimize voltages and current drawn by the circuit. Since our circuit must operate on two AAA batteries, the voltage criterion was a slight problem. Two AAA batteries produce a combined voltage of 3 V. Since our amplifier stage needed a higher voltage than 3V, we had to include an additional stage in our design.

Secondly, when ordering parts to prototype the circuit, we tried to search for the cheapest available parts. Typical single unit prices were significantly more than 100 unit list prices. Therefore, we used 100 unit list prices for materials cost.

3 PROJECT DESIGN AND IMPLEMENTATION

Our project design can be divided into two sections: amplifier design, and dc-dc switching converter design.

3.1 AMPLIFIER CIRCUITRY

The final amplifier circuit used in our project was ultimately our third design approach. This section outlines our design progress beginning with a discrete transistor amplifier, an op amp -based complementary feedback amplifier, and finally an op amp -based emitter follower amplifier uniquely configured for semi- rail-to-rail operation.

3.1.1 PRELIMINARY DESIGN APPROACH

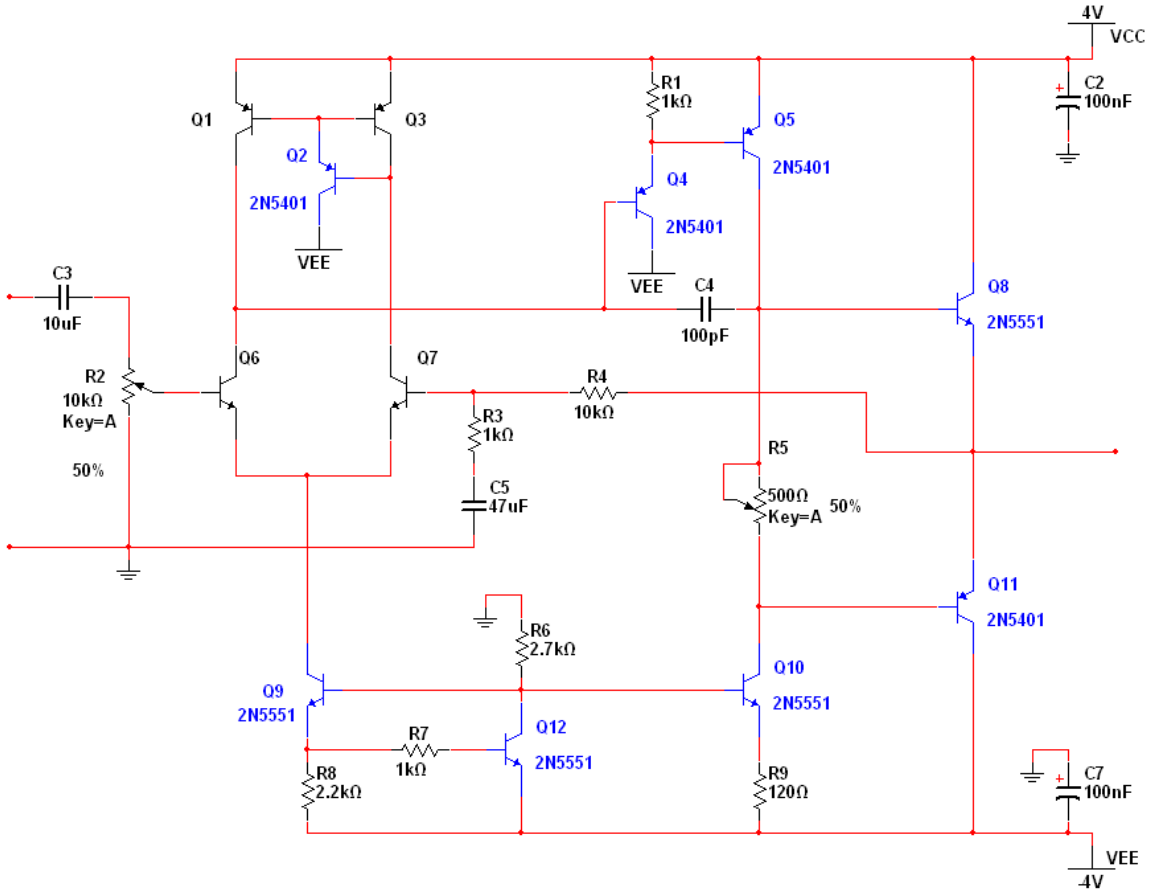


FIGURE 2 - SCHEMATIC OF DISCRETE AMPLIFIER DESIGN.
*SEE APPENDIX 7.1 FOR IMAGE OF PROTOTYPE

Our first design approach was the discrete transistor circuit of Figure 2. The focus of the first four labs led us to believe that the emphasis of this activity was on discrete amplifier design. The differential input stage was designed using monolithic transistors packaged in the CA3096. The NPN devices (Q6, Q7) have higher gain than the PNP devices (Q1, Q3) so we selected them for use

as a differential amplifier. Being monolithic, these transistors are very well matched which leads to good common-mode rejection (CMR) in the input stage. The monolithic PNP transistors (Q1, Q3) are also very well matched so we used them in the current mirror active load circuit. Due to the relatively low gain of the PNP devices, employing them in a simple two-transistor current mirror would result in a small, but significant, asymmetry in the diff-amp collector currents. Good CMR in a differential amplifier requires accurate matching of collector currents, and in our case, collector current symmetry would likely be the limiting factor in the amplifier's overall CMR, and therefore, in its THD performance. To improve the accuracy of our current mirror, we inserted a relatively high gain transistor, Q2, to greatly reduce the impact of the Q1 and Q3 base currents on Q3 collector current.

Q12 generates a 1.3V reference (V_{CE9}) that is used by Q9 and Q10 to form Widlar constant current sinks for both the diff-amp stage and voltage amplifier stage, respectively. The diff-amp's constant tail current, regulated by Q9, is 300μA which leads Q6 and Q7 to exhibit their maximum h_{FE}. The voltage amplifier's constant collector current is programmed by R9 to be approximately 4mA. We chose 4mA to ensure there would be enough base current for the output transistors during high-power operation. Transistors Q8 and Q11 form an emitter follower output stage biased at the edge of the class B region using R5 to generate V_{BIAS} = 1.2V. At this bias voltage, the output transistors are on the verge of conducting, which allows for relatively low crossover distortion while the output stage is still in class B mode with quiescent current through Q8 and Q11 equal to zero.

This design yielded very low THD (<0.032% @ P_L=100mW, f=1kHz) but is not very efficient because it requires a ±4V supply to produce a 2.53V peak amplitude output signal. The factor determining our peak output amplitude is the amplifier's negative voltage swing limited by the Widlar current source, Q10, of the voltage amplifier stage.

As stated previously, the topics of the first four labs in this course led us to assume that the final course project would be to apply the concepts learned in lab by developing a full amplifier solution to meet the given specifications. Below is an excerpt from the Team Project Specifications document that addresses the matter of purely discrete designs versus designs incorporating commercial ICs.

"… the use of commercial ICs specifically designed as headphone amplifiers **is not** permitted, even though there are a number of ICs that might work in this application. Part of the project learning experience is to determine the best internal architecture for a good stereo headphone amplifier, so discrete transistors or op amps are allowable but integrated headphone amplifier ICs are not."

Against all probability, each member of our team somehow managed to overlook those two little words, "op amp." Fortunately for us, there was a mid-project review conducted by Todd Marco during which he informed us that op-amps were indeed permitted. He was also excited to see that we had made so much progress with a discrete transistor design. He noted that it would be "kind of cool" if we used a discrete amplifier design in our final project, at which point one of our teammates quipped and said "yeah, it would be kind of cool, but it would also be kind of cool if we won the ten bonus points for lowest power consumption."

Despite how much many of us enjoy designing and perfecting discrete amplifier circuits, it was clear that if we wanted the ten bonus points, we would have little chance of competing if other teams were utilizing the high performance and low power consumption of commercial op amps. So after

spending the first several weeks on what turned out to be a lost cause, we chose to start again from scratch on a design that would instead incorporate a low-power op amp.

3.1.2 SECOND DESIGN APPROACH

Our final design approach was to use an op amp as a voltage amplifier and a discrete transistor output stage as a buffer to supply the 79mA peak output current to the 32Ω load. Our criteria for op amp selection was aimed at minimizing supply current, and there are a wealth of op amps available with very low supply currents, but we had to make sure our op amp was rated with an appropriate slew rate. Of the op amps that met our slew rate requirement (SR ≥ 0.318V/µs), we selected the device that had the lowest supply current and a supply voltage range appropriately suited to our application. Our final choice was the MAX4332 dual rail-to-rail op amp with a SR = 1.5V/µs, a quiescent supply current of 275µA per amplifier, and an operating supply voltage range of 2.3V to 6.5V.

With the main goal of minimizing power consumption, it became clear to us that the winning design in this competition would be one composed of power amplifiers with rail-to-rail outputs. Based on the design specifications, each amplifier must be able to meet the peak output requirement of ±2.53V @ ±79mA. In an emitter follower output stage with $V_{BE(ON)}$ = 0.7V, the minimum supply voltage must be ±3.23V, and the peak power consumed by the output stage would be $|3.23V|x|55.9mA_{RMS}|$= 181mW. In an output stage with the same peak output requirements, but in which the output could swing to within 100mV of the supply rails, then the peak power consumption would be $|2.63V|x|55.9mA_{RMS}|$= 147mW. This means that a stereo headphones amp with near- rail-to-rail output swing could potentially save as much as 2(34mW) = 68mW when compared to a circuit utilizing traditional emitter follower output stages. This would give us a clear advantage over the other teams, so we committed ourselves to the design of a rail-to-rail output stage.

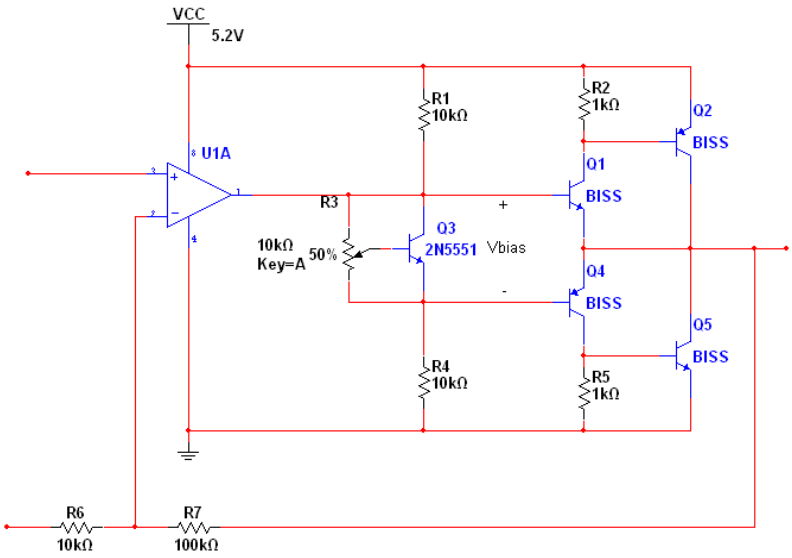


FIGURE 3 - COMPLEMENTARY FEEDBACK OUTPIT STAGE DESIGN
*SEE APPENDIX 7.2FOR IMAGE OF PROTOTYPE

Before formally beginning this design process, we knew that the voltage swing of our near- rail-to-rail output stage would be limited by the $V_{CE(sat)}$ of the transistors we use. We therefore searched extensively for transistors with very low $V_{CE(sat)}$ and discovered what are called BISS (Breakthrough In Small Signal) transistors. These devices are characterized by relatively high gain ($h_{FE} \approx 450$) and $V_{CE(sat)} \leq 100mV$ or as low as 10mV if enough base current is supplied so that I_C/I_B is reduced to a ratio value approaching 10.

After selecting our op amp and BJTs, we then began the design of a near- rail-to-rail output stage. We settled on the basic design architecture of Figure 3Figure 2**Error! Reference source not found.**, which is commonly known as a complementary feedback output stage. A more familiar designer would be quick to point out that this circuit is inherently incapable of producing a near-rail-to-rail output swing, and its output swing is actually slightly less than an emitter follower circuit. This fact would unfortunately only become known to us after spending several hours struggling to stabilize the feedback loop. Complementary feedback designs are often prone to instability due to the a combined effect of output stage transistor junction capacitances and a tendency toward output phase reversal during clipping which can lead to catastrophic self-sustained oscillation. As we began to see improved stability in our design, we also realized its inherent output swing limitations and had to scratch the idea all together.

We had encountered a serious roadblock that threatened to unravel our potentially winning strategy of minimizing power consumption in the output stage. However, with the use of high quality BISS transistors along with some imaginative design work, our team was able to overcome this obstacle and achieve some of the power saving benefits of a rail-to-rail output stage while using a simple and reliable emitter follower circuit.

3.1.3 FINAL DESIGN

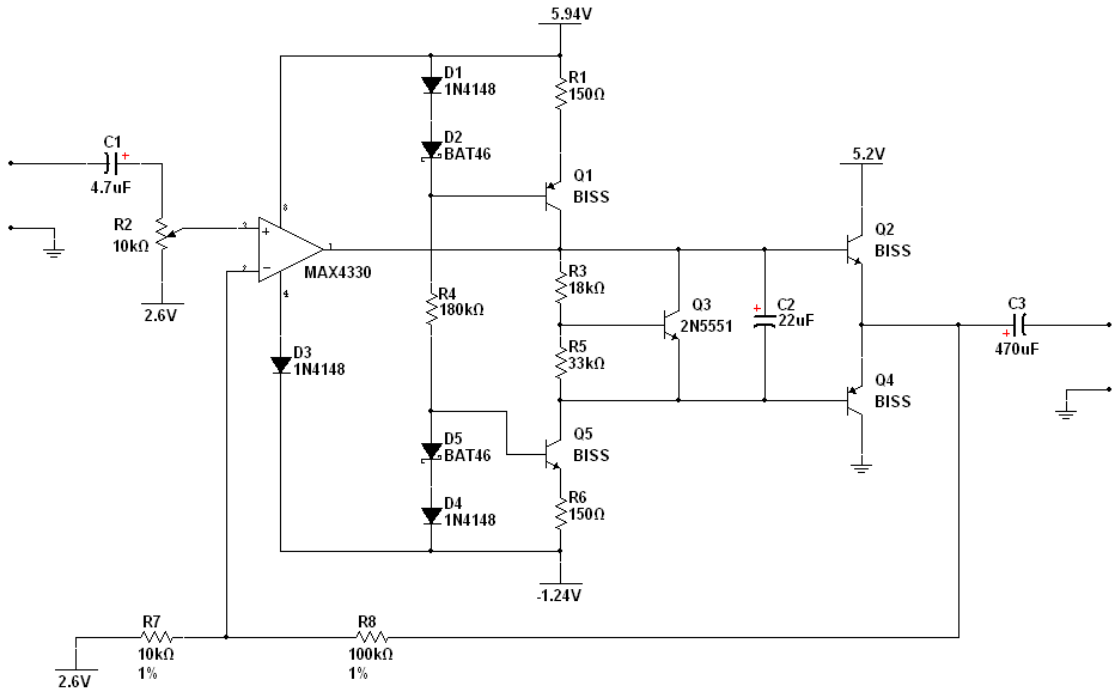


FIGURE 4 - FINAL DESIGN OF THE AMPLIFIER MODULE

Our final power amplifier design is shown in Figure 4. A conventional emitter follower output stage is typically powered by supply voltages that are at least one V_{BE} drop above the peak output voltage. In our circuit we realized that yes, the positive and negative output voltage swing is limited by the maximum voltage that can be applied to the corresponding base terminals of the output transistors. However, to achieve a given output swing, what is the minimum voltage magnitude that must be supplied to collector terminals?

Since the output voltage is generated on the emitter terminals, and the minimum collector-emitter voltage is $V_{CE(sat)}$, then in order to achieve a given output voltage, the emitter follower's collector terminals need only be supplied with a voltage magnitude of at least $V_{OUT(max)} + V_{CE(sat)}$. Therefore, our output stage can be supplied with ±2.6V rails and produce a peak output swing of ±2.53V, as long as the base terminals of Q2 and Q4 can be driven to a magnitude one diode drop ($V_{BE(on)}$) above $V_{OUT(max)}$. With this design approach and very low $V_{CE(sat)}$ transistors, we can achieve the nearly 70mW combined power savings in our final stereo amplifier compared to traditional approaches in which both the output stage and voltage amplifier stage share the same supply rails. In the end, this design strategy would give us a unique advantage above the other teams and would essentially guaranteed our success in achieving the lowest power consumption in the 2009 EE 410 circuit design competition.

Referring to Figure 4, the output of the op amp is connected to the amplified diode circuit of Q3, R3 and R5. The amplified diode circuit generates the 1.1V bias voltage for the B-E junctions of Q2 and Q4. With V_{BIAS} = 1.1V, the quiescent collector current through Q2 and Q4 is virtually zero, but any movement of the op amp output voltage will turn on one of the devices allowing for low crossover distortion while maintaining class B operation with no power wasted in Q2/Q4 bias current.

The amplified diode circuit is positioned in the 500μA current path created by the Q1 and Q5 constant current source and sink. These Widlar circuits permit only a small current to be sourced and sunk from the supply rails during operation, and they also ensure that the constant current is maintained during large voltage swings. This technique saves power compared to a simple resistor network, and also maintains the current sourcing and sinking even when the op amp output voltage approaches the rails. When the op amp's output approaches the a rail, the additional current adds to the base current of the "on" output transistor to further reduce VCE(sat) and improve rail-to-rail operation. C2 serves as a charge reservoir to also assist in providing base current to the "on" transistor when V_{OUT} approaches the rails.

Diode pairs D1, D2, and D5, D6, provide approximate 0.6V references for the Q1 and Q5 Widlar circuits. The current through this reference-setting path is limited to 40μA by R4, and these same 0.6V references are also used for the Widlar circuits of the second audio channel, eliminating the need for another 40μA current path. The MAX4330 consumes approximately 275μA per amp and has an operating supply limit of 6.5V, and an absolute max of 7V, so because the negative dc-dc converter could not be programmed to less than 1.24V, diode D3 has been placed in the negative supply path of the op amp to ensure the max supply voltage is not exceeded.

The complete circuit is configured as a non-inverting amplifier with 20.8dB voltage gain programmed by R7 and R8. Precision 1% metal film resistors were used to increase the gain accuracy between of both audio channels so that both outputs can be simultaneously driven to max power from the same □10dBV input for the purpose of power consumption measurements. Stereo volume can be adjusted from zero to full power using the ganged potentiometer R2. Input coupling capacitor C1 forms a low frequency cutoff with R2 near 3.4Hz, and there is another low frequency

cutoff near 10.6Hz created by the output capacitor C3 and 32Ω load resistance. We considered introducing a dominant high frequency cutoff point to reduce the noise contribution of the switching inverters, but high frequency noise was not a problem in our circuit so we permitted our bandwidth to extend far beyond the audio spectrum.

As evident in Figure 4, our amplifier output stages are operating from a single supply 5.2V source. This is 5.2V supply powers both output stages of the stereo amplifier and therefore supplies the vast majority of the amplifier's overall power consumption. It is for this reason that we chose to generate a single supply because a single 3V to 5.2V boost converter circuit tends to be available with a higher efficiency than what could be achieved in a ±2.6V dual converter circuit. The reduced efficiency of a bipolar supply converter circuit is largely due to the inverting converter which contains a charge-pump stage. Efficiency is most important in the converter used for the output stages, but for the op-amp voltage amplifier and base-drive circuit, power consumption is so small that the efficiency of the converters generating the -1.24V and 5.94V was not our primary concern.

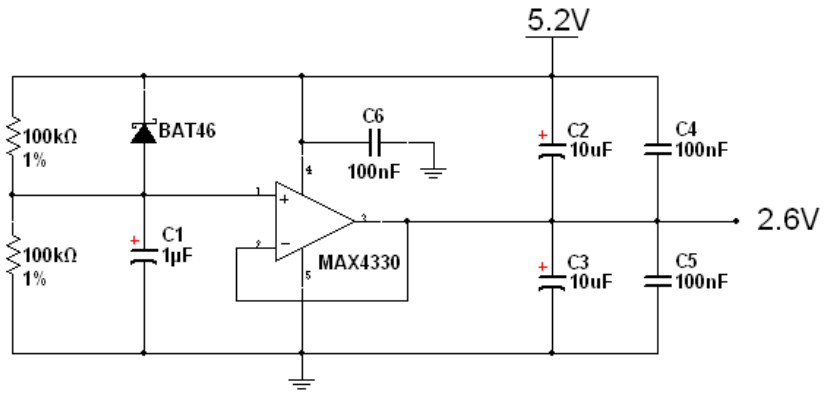


FIGURE 5 - 2.6V REFERENCE GENERATOR

The 2.6V reference potential for the audio signals is generated by the circuit of Figure 5. The circuit uses another MAX4330 op amp as a voltage follower capable of regulating the ½ supply reference generated by the precision resistor voltage divider at the non-inverting input terminal. Electrolytic capacitors C2 and C3 provide additional filtering and reservoir charge storage for any sudden current demands. C4 and C5 perform the same function as C2 and C3, but with improved performance at higher frequencies.

Capacitor C1 has been introduced to soften the turn-on transient caused by the sudden rise time of the 2.6V reference potential. With C1 positioned as shown, the voltage at the non-inverting input terminal (and thus, the 2.6V audio reference) is slower to rise to the full 2.6V value because of the resultant 50ms RC time constant. Below are two plots of the turn-on transient across a 32Ω load resistor when C1=1µF is included, and when C1 is omitted. The turn-on transient is significantly suppressed by C1, and this manifests itself as a much softer "pop" noise in the headphones when power is applied to the circuit. It should be noted that we did not investigate the turn-off transient of our circuit. The effect of C1 on the output turn-on transient is shown in Figure 6**Error! Reference source not found.** and Figure 7**Error! Reference source not found.**.

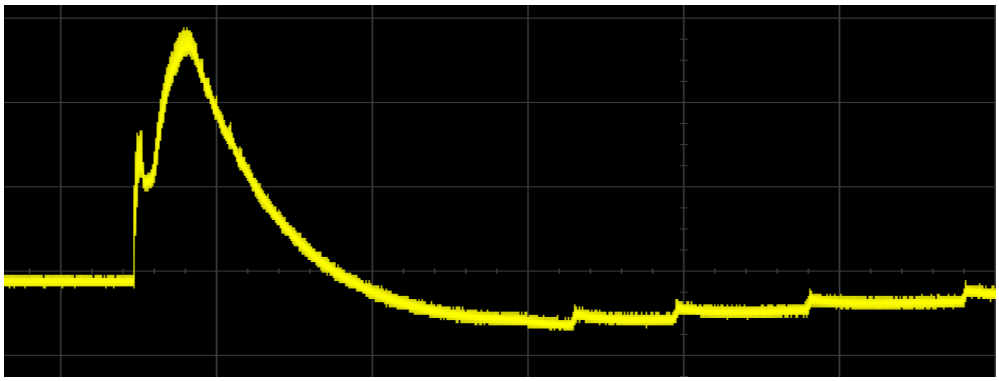


FIGURE 6 - WITHOUT C1 CAPACITOR (100MV/DIV)

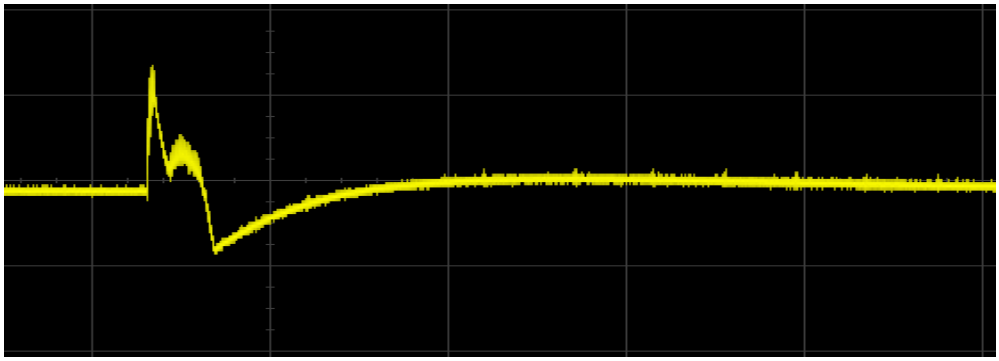


FIGURE 7 - WITH C1 CAPACITOR (100MV/DIV)

3.2 DC-DC CONVERTER CIRCUITRY

Since the input voltage is supplied by 2 AAA batteries, the maximum output voltage can only be as high as 3V without any boost. However, in order to achieve the design specification that the amplifier should have 100dB gain, the maximum required voltage will excess 3V. Therefore, we include three DC-DC convertors designs in our final implementation. Among them, one is to generate the Vcc voltage of 5.94V, one is to generate the Vee voltage of -1.24V, and the other is used to generate the 5.2V voltage for the proposal of half voltage generator.

We chose three different types of DC-DC converters from Linear Technology. LT1615 is a boost-up converter to generate the 5.94V Vcc voltage, LT1617 is a inverter converter to generate the -1.24V Vee voltage, and LTC3429 is another boost-up converter that can provide sufficient output driving capacity. The schematic of these three converters are shown in Figure 8.

The core design of the converter is referred to the datasheet provided by Linear Technology. In addition, we added both electron and ceramic capacitors at the both the input and the output terminals of the DC-DC converter circuitry to decouple both the low-frequency and high-frequency noises on the power rails.

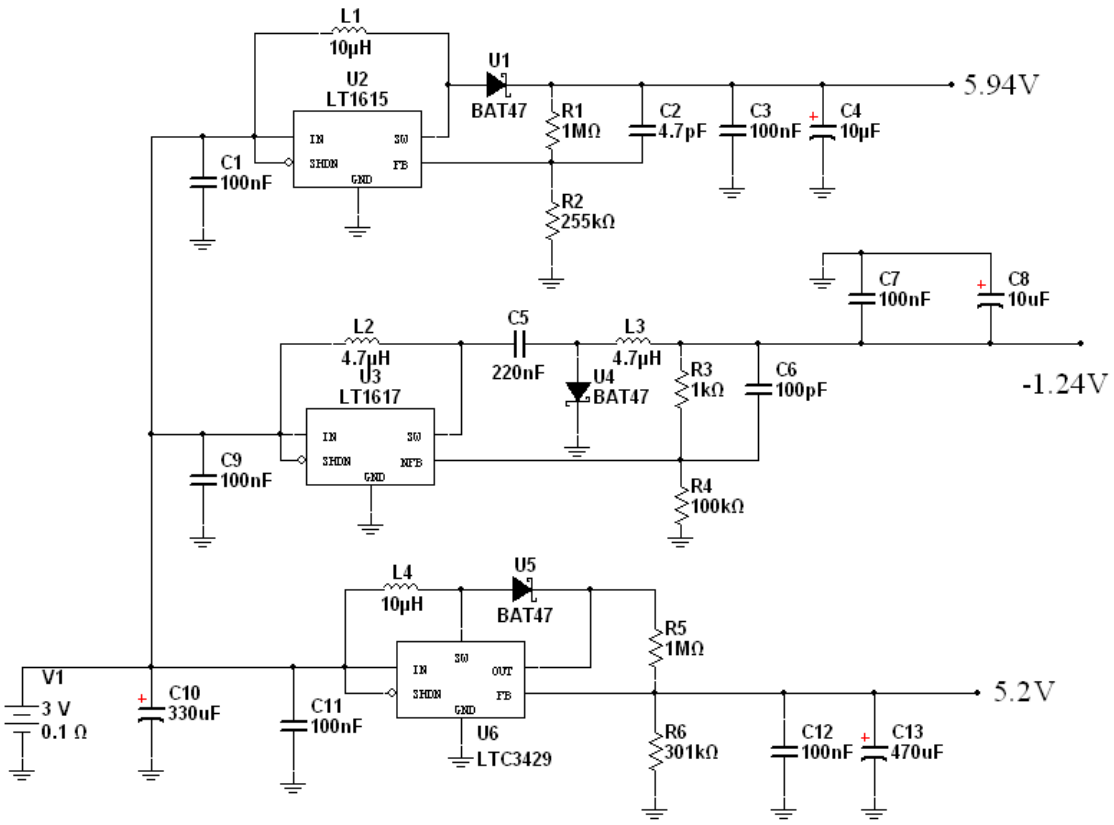


FIGURE 8 – THE SCHEMATIC OF 3 DC-DC CONVERTER DESIGNS

4 MEASUREMENT

4.1 NOISE MEASUREMENT

In our design implementation, there are two main noise sources. The three DC-DC converters used in our design are all based on switched-mode conversion. This conversion method is more power efficient (often 75% to 98%) than linear voltage regulation, but the drawback is that it will introduce switching noise. Besides DC-DC converters, the other circuitry components introduce electronic noise, which is unwanted but inevitable signal character of all electronic circuits.

4.1.1 SWITCHING NOISE

We use AC coupling mode to detect the switching noise on the power plane generated by DC-DC converters. The measurement is shown in Figure 9.

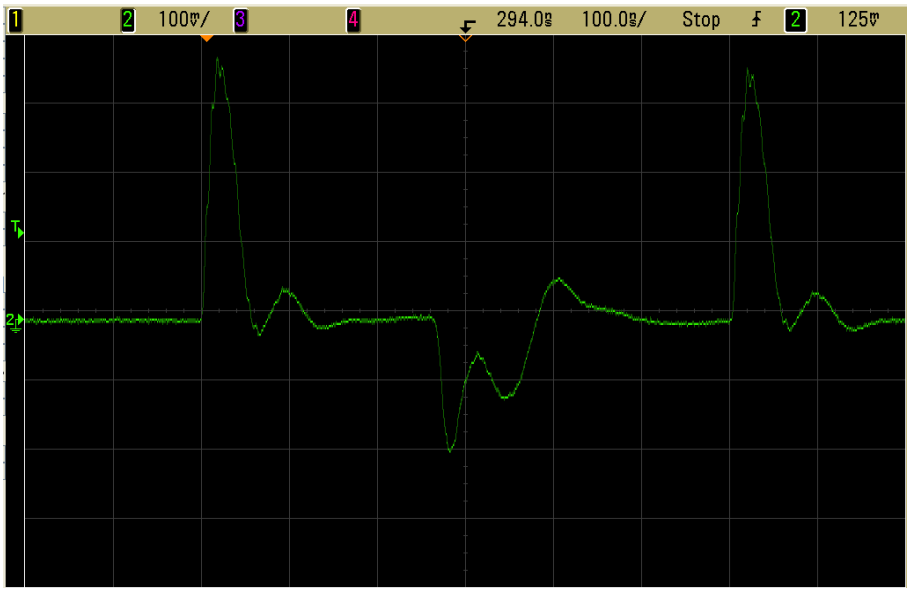


FIGURE 9 – SWITCHING NOISE MEASURED ON POWER PLANE.

The measured period of the switching noise is

$$\tau = 600 \text{ ns}$$

Therefore, the switching noise frequency is about

$$f_{switching} = \frac{1}{\tau} = \frac{1}{600 \text{ ns}} = 1.67 \text{ MHz}$$

This switching noise frequency is well consistent with the DC-DC converter datasheet, and it is far away from the audio frequency, which is usually below 44 KHz.

4.1.2 SPOT NOISE DENSITY

The specification on the spot noise density is below $-128\text{dBV}/\sqrt{\text{Hz}}$. To measure the spot noise density, we use the HP Signal Analyzer 3561A to observe the power spectrum. In addition, the noise density is measured with the circuit gain adjusted to 20 dB and the inputs terminated with 1 kΩ resistors and the outputs terminated with 32Ω resistors. We set the bandwidth span of 3561A to be 400 Hz, so that the frequency resolution of the power measurement is 1 Hz (Because the frequency resolution of 3561A is 1/400 of the bandwidth span according to the specification of 3561A). A plot of spot noise density vs. frequency is measured from 20 Hz to 20 kHz.

We record the noise RMS voltage measured across the output 32Ω resistor as listed in Table 1.

Frequency (Hz)	Measured V_{RMS} on 32Ω resistors (dBV)
20	-106.62
50	-105.84
100	-103.40
200	-107.64
1K	-111.66
2K	-119.24
5K	-119.04
10K	-118.78
20K	-118.24

TABLE 1 MEASURED NOISE RMS VOLTAGE ACROSS THE OUTPUT RESISTOR

We convert the measured data to the unit of $\text{dBV}/\sqrt{\text{Hz}}$, since the noise density is defined as the RMS voltage measured on a 1Ω resistor. The translation procedure is described by using the noise value measured at 1 KHz as follows,

$$V_{\text{Output,RMS}} = -111.66\text{dBV} = 2.61\mu\text{V}$$

$$P_{\text{noise}} = \frac{{V_{\text{Output,RMS}}}^2}{R} = \frac{2.61\mu\text{V}^2}{32\Omega} = 0.213\text{pW}$$

The noise density in our case is actually $P_{\text{noise}}/1$ Hz, because we used 1 Hz as the frequency resolution. Hence,

$$P_n = 0.213\text{pW}/1\text{ Hz} = 0.213\text{pW/Hz}$$

$$V_{\text{nRMS}} = \sqrt{P_n \times 1\Omega} = \frac{0.462\mu\text{V}}{\sqrt{\text{Hz}}} = -126.71\text{dbV}/\sqrt{\text{Hz}}$$

For quick calculation, we can simply do the transformation by adding another -15.05dB on the measured voltage level. Therefore, our measured spot noise density is listed in Table 2 and plotted in Figure 10.

Frequency (Hz)	Measured V_{RMS} on 32Ω resistors ($\text{dBV}/\sqrt{\text{Hz}}$)
20	-121.67
50	-120.89
100	-118.45
200	-122.69

1K	-126.71
2K	-134.29
5K	-134.09
10K	-133.83
20K	-133.29

TABLE 2 MEASURED SPOT NOISE DENSITY

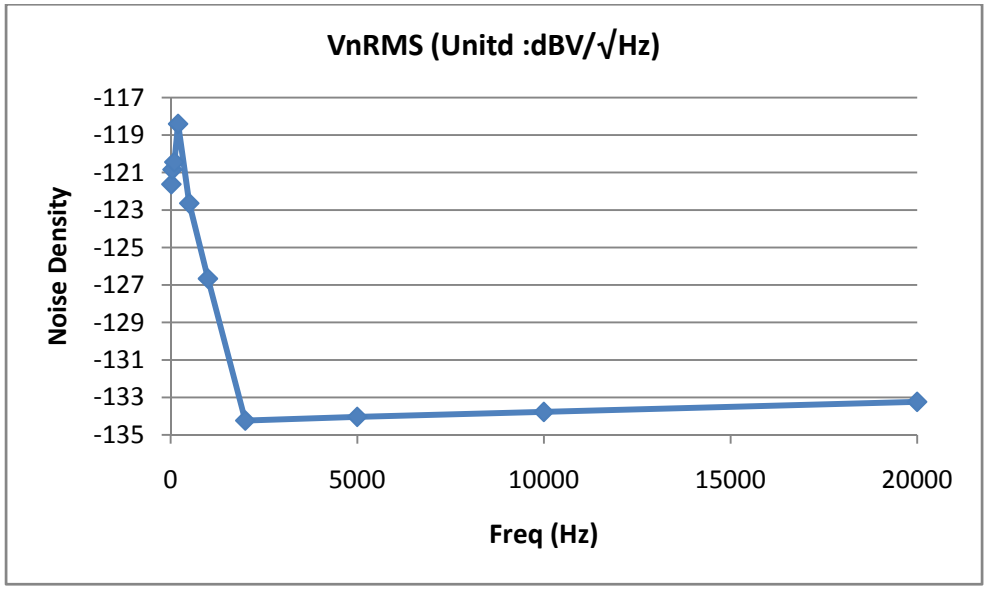


FIGURE 10 – SPOT NOISE DENSITY VS. FREQUENCY

Observing the result, we find the noise density is high in the low frequency region and it is low in the high frequency region. On average, the noise density of our circuit is well below the noise requirement, which is $-128\text{dBV}/\sqrt{\text{Hz}}$.

4.2 DISTORTION MEASUREMENT

We use the Signal Analyzer 3561A to measure the THD values. To do the measurement, we set the input frequency to be 1 KHz, and rely on the 3561A THD measurement feature to retrieve the data.

During the measurement, the number of harmonic frequency is set to 10, the frequency range is set to begin from 500 Hz with a 10 KHz span, and the measurement result is set to "peak hold".

The THD measurement is listed in Table 3.

	Left Channel	Right Channel
THD (10mW output)	0.0333%	0.0393%
THD (100mW output)	0.457%	0.506%

TABLE 3 – THD MEASUREMENT

4.3 POWER MEASUREMENT

The power consumption of the circuit was the greatest concern of the group. The goal of lowest power out of all groups was what drove the design, and led to the use of the low saturation BISS transistors. The total power consumption, when outputting 100mW to each 32Ω load (200mW total), was measured to be 371mW. That makes the circuit 53.9% (200/371) efficient.

The power loss was found by measuring the power delivered to the amplifier (287mW). From there all the other values could be calculated:

Amplifier Power Loss = 287mW – 200mW = 87mW 87mW/371mW = 23%

Converter Power Loss = 371 – 287mW = 84mW 84mW/371mW = 23%

The power break-down is shown in Figure 11.

The design uses a Class-AB output stage, and the concern was that the circuit was getting maximum efficiency from the output. Ideal efficiency from a Class-AB amplifier is 78.5%. The amplifier efficiency of our design can be calculated as 69.3% (200mW/287mW). We consider this result as satisfactory, and this almost ideal performance is due to the use of the low saturation BISS transistors.

However, a more power-efficient DC-DC converter can contribute more to the overall power efficiency of the entire design.

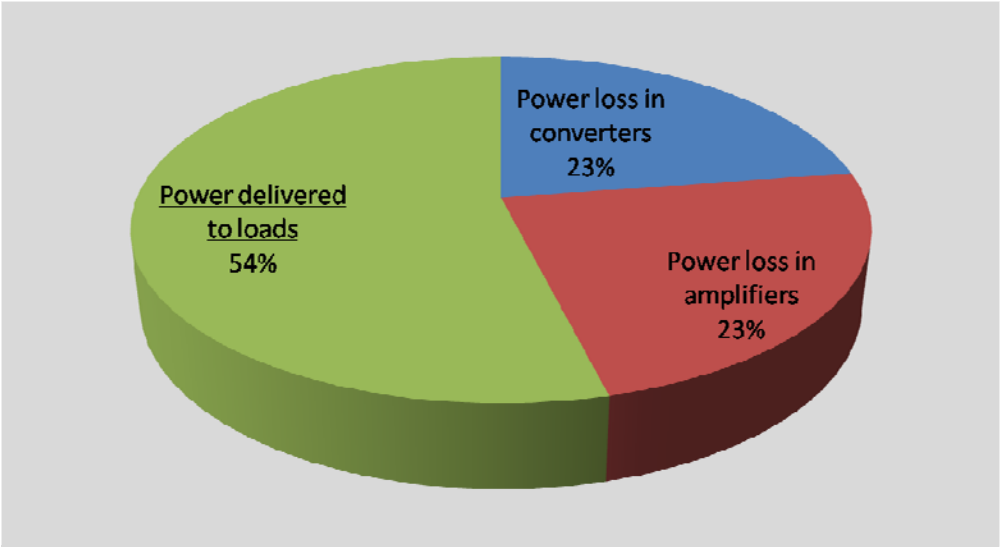


FIGURE 11- POWER BREAK-DOWN

4.4 BATTERY LIFE

The total power consumption was calculated from measuring I_{IN} during max output of 100mW being delivered to each load. Then current was multiplied by the voltage (3V) to find the power (P=IV). The battery life was not measured because there was not sufficient time to test the circuit; it would have taken over four days of constant run time. A calculation was done consistent with the

description from the project specifications, which state using an output power level 10dB below the measured maximum:

Triple A battery rating: 1250mA*hr Battery Life => 1250mA/I_{AVG}

P_{TOT} = 10 log .371W = -4.31 dB P_{AVG} = 10^ [(P_{TOT} – 10)/10] = 37.1mW

I_{AVG} = P_{TOT}/3V = 12.367mA Battery Life => 1250mA*hours/12.367mA = 101 hours

Initially the battery life was calculated incorrectly to a value around 30 hours. This concerned the group greatly because we had met the power specification and yet we were far from meeting the battery life specification of 90 hours. Immediately we thought there must be some considerable current leakage in the circuit and suspected the DC/DC converters. The thought was that the converters were using too much power even without an input signal. Basically draining the batteries when the circuit was supposed to be off and wasting wattage. The mA*hr rating of the batteries was questioned; maybe the rating found was incorrect. The solution was found from carefully reading note 5 from the specification sheet. The first interpretation of the note was that the circuit currents needed to be measured when it was using total power 10dB below the found power maximum. But the we were only meant to estimate the battery life using an average current found from a average power; average power being a value 10dB below the circuit maximum.

5 PRICE LIST

5.1 THE PRICE OF DC-DC CONVERTERS

The price of all the components used in DC-DC converter sub-module is listed below. The subtotal is $19.16.

Component name	DigiKey Part #	Manufacturer	Qty.	Cost per unit	Total Cost
LT1615 (Step-up DC-DC converter)	LT1615ES5#TRMPBFCT-ND	Linear	1	$ 3.330	$ 3.330
LTC3429 (Step-up DC-DC converter)	LTC3429ES6#TRMPBFCT-ND	Linear	1	$ 3.667	$ 3.667
LT1617 (Inverting DC-DC converter)	LT1617ES5#TRMPBFCT-ND	Linear	1	$ 3.330	$ 3.330
BAT47 (Schottky Diode)	497-3773-1-ND	STMicroelectronics	3	$ 0.460	$ 1.380
1/4 W Carbon Film Resistor	CF1/4(Value)%5RCT-ND	Stackpole Electronics, Inc.	4	$ 0.019	$ 0.076
1/4 W Metal Film Resistor	(Value)XBK-ND	Yageo	2	$ 0.037	$ 0.074
Radial Aluminum Electrolytic Capacitor					
10 uF	P5567-ND	Panasonic	2	$ 0.077	$ 0.154
330 uF	P5573-ND	Panasonic	1	$ 0.260	$ 0.260
470 uF	P5585-ND	Panasonic	1	$ 0.492	$ 0.492
Ceramic Chip Capacitor					
4.7 pF	478-1159-1-ND	AVX	1	$ 0.124	$ 0.124
100 pF	399-1122-1-ND	Kemet	1	$ 0.057	$ 0.057
100 nF	399-1096-1-ND	Kemet	6	$ 0.012	$ 0.070
220 nF	399-1103-1-ND	Kemet	1	$ 0.183	$ 0.183
Inductor 10uH	308-1311-1-ND	SUMIDA	2	$ 1.490	$ 2.980
Inductor 4.7uH	308-1317-1-ND	SUMIDA	2	$ 1.490	$ 2.980

TABLE 4 – THE PRICE OF THE COMPONENTS USED IN DC-DC CONVERTERS

5.2 THE PRICE OF AMPLIFIERS

The price of all the components used in amplifier sub-module is listed below. The subtotal is $16.01.

Component name	DigiKey Part #	Manufacturer	Qty.	Cost per unit	Total Cost
MAX4332	MAX4332ESA+-ND	Maxim	2	$ 3.450	$ 6.900
BAT46	497-5559-1-ND	STMicroelectronics	5	$ 0.211	$ 1.056
1N4148	568-1360-1-ND	NXP Semiconductors	5	$ 0.010	$ 0.052
PBSS4350X (NPN transistor)	568-4159-1-ND	NXP Semiconductors	4	$ 0.450	$ 1.800
PBSS5350X (PNP transistor)	568-4170-1-ND	NXP Semiconductors	4	$ 0.600	$ 2.400
2N5551RLRAGOSCT-ND (NPN Transistor)	2N5551RLRAGOSCT-ND	ON Semiconductor	2	$ 0.185	$ 0.370
Radial Aluminum Electrolytic Capacitor					
1 uF	P5563-ND	Panasonic	1	$ 0.077	$ 0.077
4.7 uF	P5566-ND	Panasonic	1	$ 0.069	$ 0.069
10 uF	P5567-ND	Panasonic	2	$ 0.077	$ 0.154
22 uF	P5568-ND	Panasonic	2	$ 0.068	$ 0.136
470 uF	P5585-ND	Panasonic	2	$ 0.492	$ 0.984
Ceramic Chip Capacitor					
100 nF	399-1096-1-ND	Kemet	3	$ 0.012	$ 0.035
1/4 W Metal Film Resistor	(Value)XBK-ND	Yageo	12	$ 0.037	$ 0.444
1/4 W Carbon Film Resistor	CF1/4(Value)%5RCT-ND	Stackpole Electronics, Inc.	4	$ 0.019	$ 0.076
10KΩ Pot	P2U4103-ND	Panasonic	1	$ 1.460	$ 1.460

TABLE 5 – THE PRICE OF THE COMPONENTS USED IN AMPLIFIERS

5.3 TOTAL PRICE

All these cost were calculated figuring each part would be bought at the 100 part price. One may notice that in some cases a metal film resistor was used in the circuit even though it is six times more expensive than a normal carbon film resistor. The reason for this goes to the fact that performance was an issue in certain cases and the circuit required a precise resistor value. One solution would be to use several cheap resistors to form a resistor network that was effectively precise but the main problem there is that now you are using numerous resistors instead of one, which would once again drive up the cost. The most inexpensive choice, while meeting the performance we wanted, was buying one high performance resistor.

Not included in either cost chart is the cost of a jack and plug ($1.81), to connect an input signal and connect an output to a pair of headphones. Their inclusion makes the total cost of the circuit $36.98. This meets the specification of a minimum use of $40 and means the circuit is within 10% of the goal.

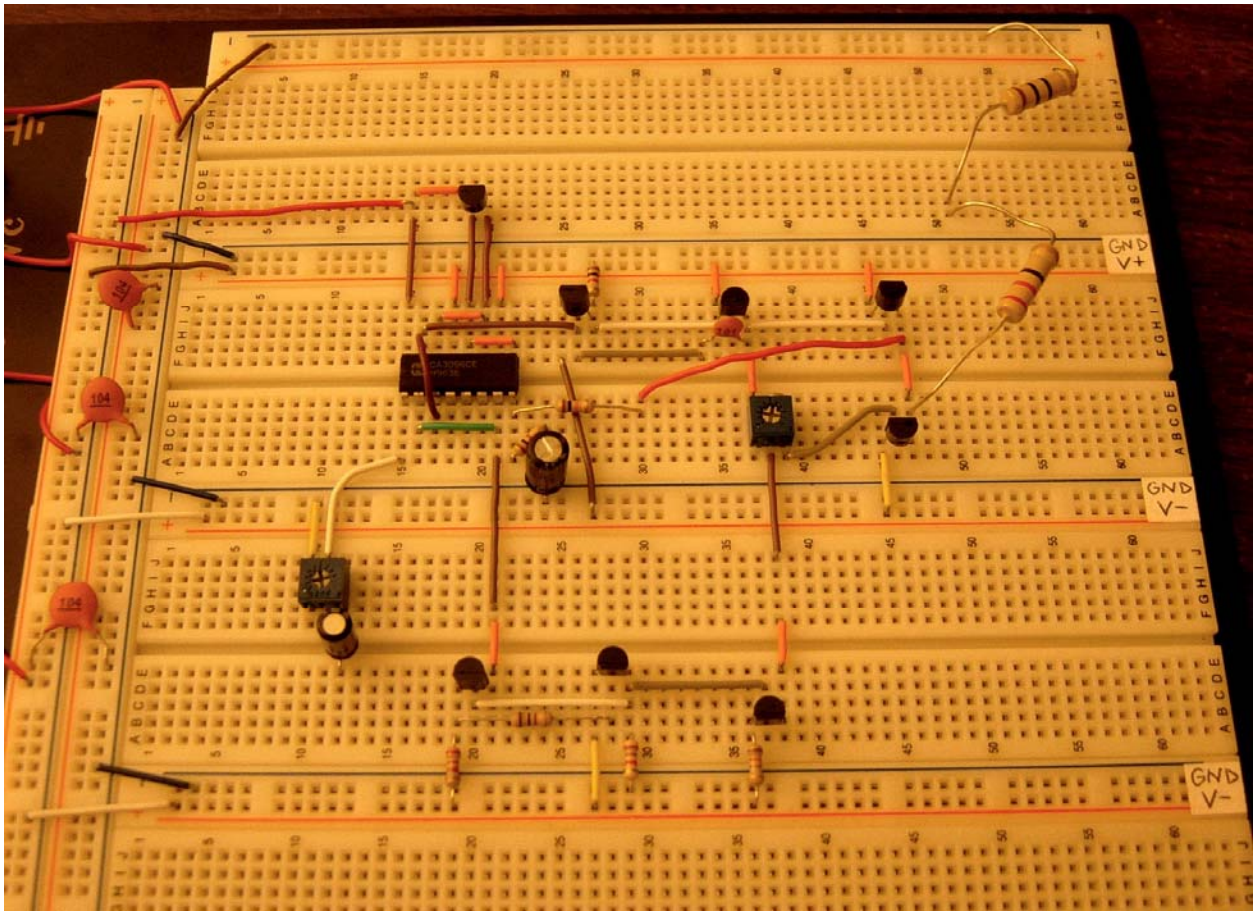
6 CONCLUSION

This project has been a very valuable learning experience for our entire team. We were able to accomplish the objectives that were set for us as well as goals that we set for ourselves. Our initial objectives were to achieve a lower than specified power consumption and materials cost. We were able to accomplish both objectives with a power consumption of 371 mW and materials cost of $36.98.

As stated earlier, the final measured efficiency at max output power was 54%, with 23% of power being dissipated in the class B amplifiers, and the remaining 23% being lost in the dc-dc converter circuitry. Thus for the future, we would like to improve on a few aspects of the design. First, lower quiescent power consumption of the circuit. This would inevitably improve on our earlier goal regarding power consumption. Accomplishing this would involve altering the circuit such that two of the DC-DC converters would power off when the output voltage is below a certain level. The circuit would then be powered from 0 – 5.2V. Next, purchase more efficient converters. Our DC-DC converters had a lower than expected efficiency. Finally, reduce the remaining noise in the circuit as much as possible.

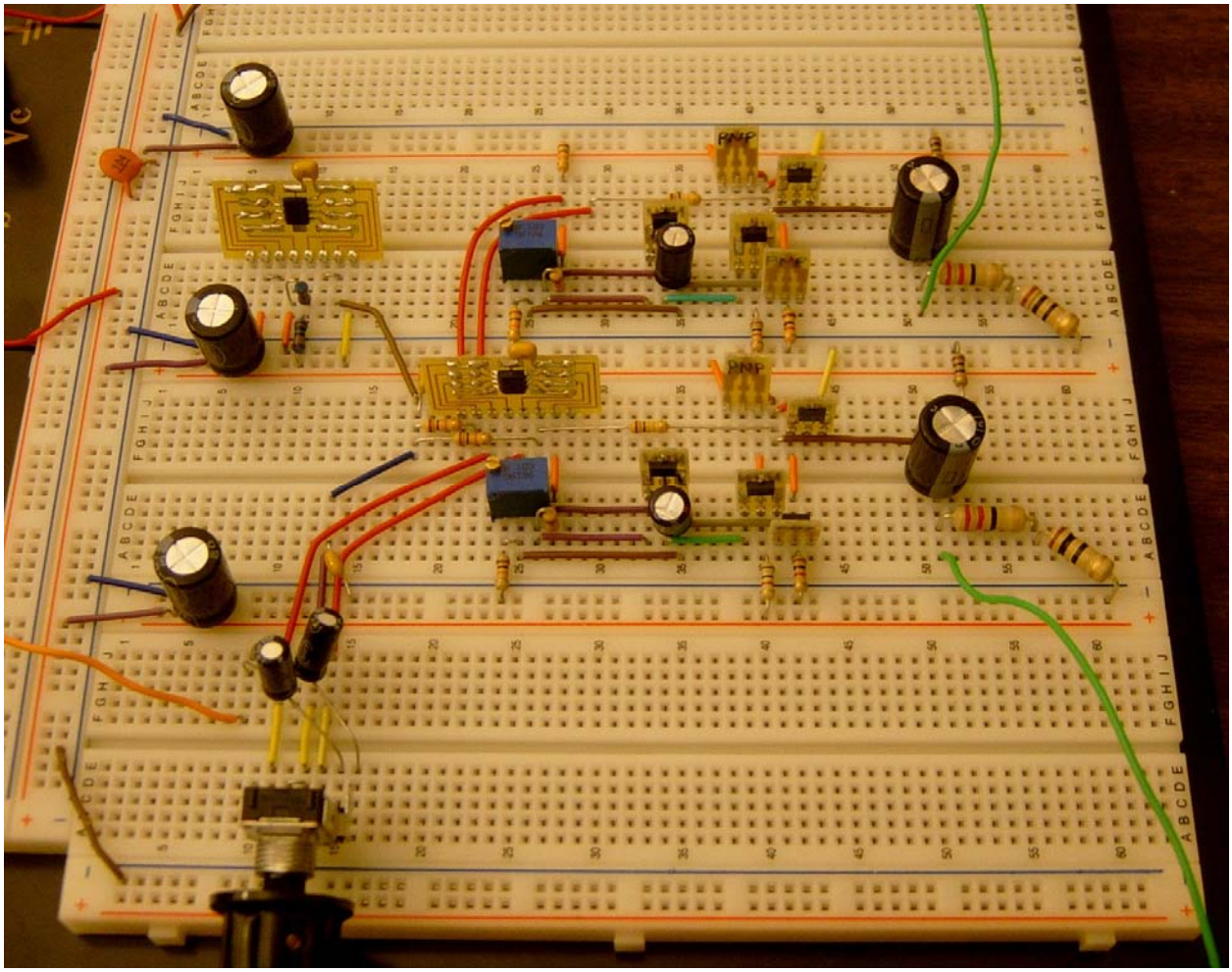
7 APPENDIX

7.1 AMPLIFIER DESIGN – VERSION 1



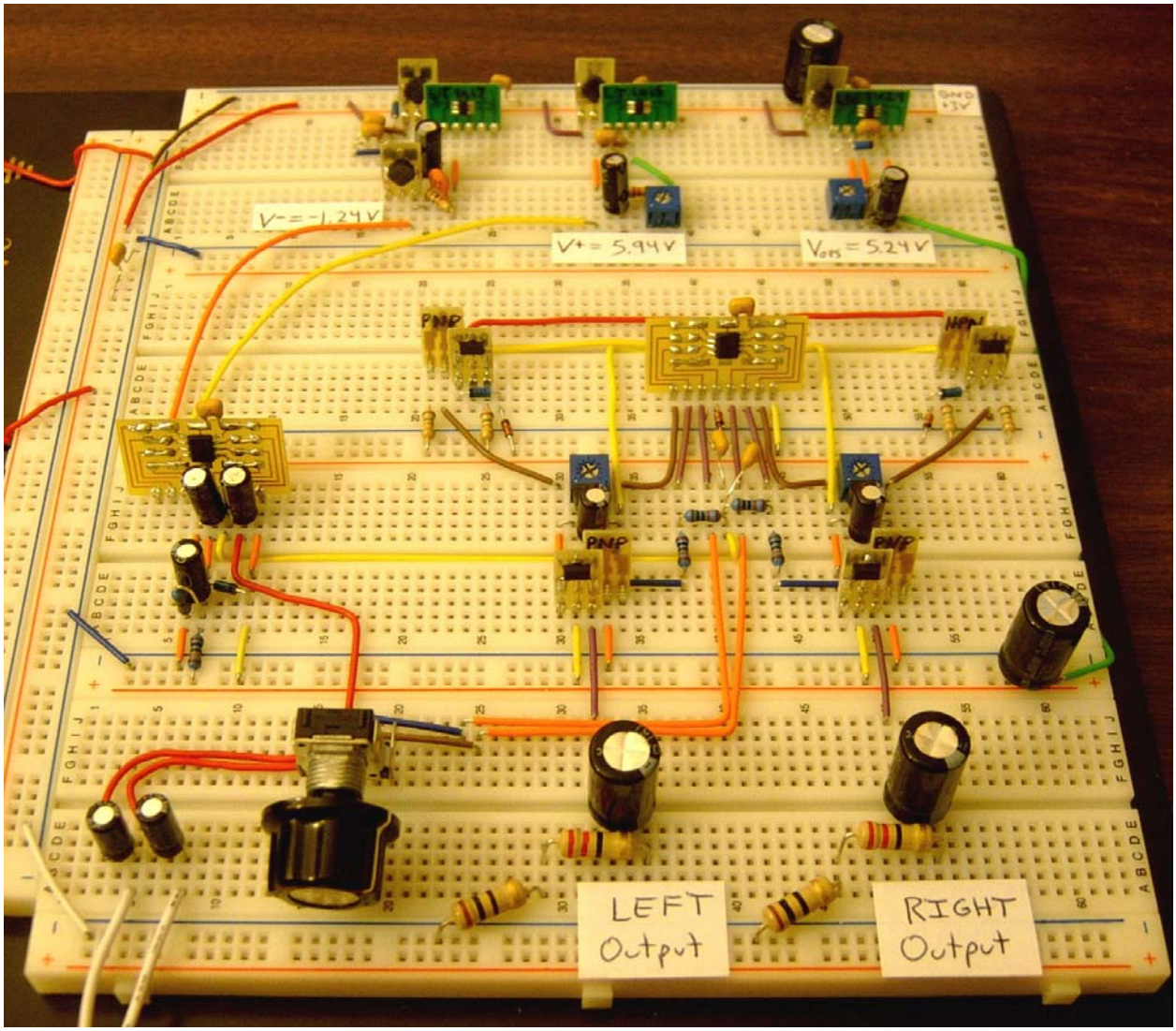
Discrete Amplifier Prototype – March 22, 2009

7.2 AMPLIFIER DESIGN – VERSION 2



Complementary Feedback (Stereo) Amplifier Prototype – April 11, 2009

7.3 FINAL PROJECT PROTOTYPE



Final Headphones Amplifier –two 100mW power amplifiers and three dc-dc converters